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Abstract
There are two categories in the digital world: synchronous and asynchronous; they are distinguished based on their synchronization, sequencing, and communication operations. All synchronous digital systems follow two fundamental assumptions. First, all signals are binary (0 and 1). Second, all components share a common referencing signal (usually a global clock) with a discrete notion of time. In asynchronous VLSI chip, either a global clock or multi-domain clocks are utilized to govern the whole system. This clocking technique works well and has dominated the electronic market for years. However, the use of clocking technique causes several increasingly challenging problems, such as clock skew, power consumption, worst-case timing assumption, electromagnetic interference (EMI) and noise, interfacing with external devices, and modularity.
Delay elements play very important role in many VLSI applications. A specific example, self-timed circuits, draws us more attention than the others. Three essential properties of being tunable, asymmetric, and post-chip alignment are very crucial for being a matched delay when building the self-timed bundled-data component.
We propose a post-chip adjustable delay element, which is low power dissipation, environment invariant, and less errors in fabrication. Delay element could be programmable, post-chip adjustable, reusable in layout template. We used TSMC 0.35um and 0.18um respectively in our circuit implementations, and further constructed our circuit layout for the post-layout simulation, and established a complete characteristic table. However, this asymmetric delay element is not merely limited to asynchronous VLSI applications, but may be applied to the synchronous as well.
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